MDE based FPGA physical Design
Fast prototyping with Smalltalk

Ciprian Teodorov, Loïc Lagadec
Loïc.lagadec@univ-brest.fr
Lab-STICC MOCS UMR 3192
FPGAs

“Flexible” hardware
Time to market

Hard to program
Hard to debug

Compute node

LUT

LUT

µP

E/S

Programmable interconnection
FPGAs

“Flexible” hardware
Time to market

Hard to program
Hard to debug

EDA required!

• C to circuit
• Debug
• Benchmarking
Our Smalltalk-based EDA legacy
Early developments (MADEO) started in 1996

Fast evolving domain (Moore + Murfy)

Refactoring is not enough to keep in the race

We have to re-design our framework
New direction

- We need to shift from
  - a generic solution to be tailored on demand
- To
  - a repository of model, algorithms, components
- In order to deliver
  - Performances
  - Scalability
  - Flexibility
  - Durability
Front end

- High level synthesis (compilation)
- Ressources allocation (logic synthesis)
Programming an FPGA in 4 steps

1. Application Model
2. Partitioning
3. Floorplanning
4. Architecture Model
5. Placement
6. Routing
7. Placed And Routed Architecture
ADL Based EDA generators

Application

Synthesizer
P&R
Bitstream generator
HW Prototype
Configuration Controller
Testbenches

Synthesis/Compilation
Simulation
Simulation
Validation
Validation

Architecture specification
ADL Description

CoWare
The ESL Design Leader

TARGET
The ASIP Company

Specifications
Architecture
Architecture specification
ADL
Description

Spécification
Architecture
Architecture specification
ADL
Description

ADL Based EDA generators
Our flow

Resources

ADL Description

Zone

Reconfigurable zones description

Context

Behavioral code

Bitstream model

Resource model

Configuration model

Prototype

Bistream

Architecture VHDL

Configuration controller

Simulation & synthesis
Some examples
RE-DESIGN
Goal oriented view extraction
Tool engine
Models as common vocabulary
Combinational circuit modeling
Target modeling
Re-design / copy down

Old Model

New Model
Isomorphic with the old model

Result of the copy down refactoring process
CONCLUSION
Let's try to summarize

- Succes: target, tool flow
Conclusion

Future work:
- Tools integration (eg Mondrian integration)
- Performances improvement
- Test coverage
- Algorithm pick and play GUI

Thank you for your attention